DIGITAL PHASE-LOCKED LOOP COMPILER

CROSS-REFERENCE TO RELATED APPLICATION

This application claims the priority benefit of Taiwan application serial no. 90126238, filed October 24, 2001.

BACKGROUND OF THE INVENTION

Field of Invention

[0001] The present invention relates to a phase-locked loop compiler. More particularly, the present invention relates to a digital phase-locked loop compiler.

Description of Related Art

[0002] Fig. 1 is a block diagram showing a conventional analog phase-locked loop device. A conventional analog phase-locked loop device, comprises: a divider 102, 112, and 114, a phase-frequency detector 104, a comparator 106, a low pass filter 108, and a voltage control oscillator 110. The signal of a conventional analog phase-locked loop is analog and therefore phase-locking must be achieved through continuous adjustment of the analog signal. Hence, the phase-locking time is longer. Furthermore, the low-pass filter in a conventional analog phase-locked device often occupies as much as 80% of the area. With the filter occupying such a large area, it is inconvenient to add other circuits such as a

built-in self-tester (BIST) around the phase-lock loop. In brief, a conventional analog phase-locked loop has the following disadvantages:

1. Latch-up time of the analog phase-locked loop is too long.

2. A low-pass filter that occupies too much of the available surface area is required.

3. The incorporation of a BIST and other circuits on the phase-locked loop device is difficult.

SUMMARY OF THE INVENTION

[0003] Accordingly, one object of the present invention is to provide a digital phase-locked loop compiler capable of improving the latch-up time and the problem of a low-pass filter occupying too much area in the circuit so that the incorporation of BIST or other circuits are facilitated.

[0004] To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, the invention provides a digital phase-locked loop compiler. The digital phase-locked loop compiler comprises: a pre-divider, a phase digital converter, a digital-to-analog voltage converter, a voltage-control oscillator, a high frequency oscillator, a post-divider, an out-divider, and a built-in self-tester. The pre-divider divides down an input frequency into a comparable input frequency according to a pre adjusting value. The phase digital converter couples with the output of the pre-divider to output a phase adjusting value according to the comparable input frequency, the feedback frequency, and a sampling frequency. The digital-to-analog voltage converter couples with the output of the phase digital converter to output an adjusting voltage according to the phase adjusting value. The voltage-control oscillator

couples with the output of the digital-to-analog voltage converter to output an output frequency according to the adjusting voltage. The high frequency oscillator couples with the input of the phase digital converter to issue a sampling frequency to sample the comparable input frequency and the feedback frequency. The post-divider couples with both the input of the phase digital converter and the output of the voltage-control oscillator for dividing down the output frequency into the feedback frequency according to a post adjusting value. The out-divider couples with the output of the voltage-control oscillator for dividing down the output frequency into a desired output frequency according to an output adjusting value. The built-in self-tester couples with the output of the phase digital converter to test the phase digital-locked loop according to the phase adjusting value.

[0005] In the first embodiment according to the present invention, the phase digital converter mentioned above comprises a phase-frequency detector, an up-down converter, and an arithmetic logic unit. Wherein, the phase-frequency detector couples with the output of both the pre-divider and post-divider to output a value-modifying signal according to the comparable input frequency and the feedback frequency. The up-down converter couples with the output of both the phase-frequency detector and the high frequency oscillator to output an adjusting signal according to the value-modifying signal. The arithmetic logic unit couples with both the up-down converter and the high frequency oscillator to output a phase adjusting value according to the adjusting signal.

[0006] Furthermore, the above sampling frequency can be 360 times the input frequency. The post-divider can adjust the necessary responsible cycle of the desired output frequency. The feedback frequency has a preset value. The phase adjusting value is a 9-bit digital signal.

[0007] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. In the drawings,

[0008] Fig. 1 is a block diagram showing a conventional analog phase-locked loop device;

[0009] Fig. 2 is a block diagram showing a digital phase-locked loop compiler according to one preferred embodiment of this invention;

[0010] Fig. 3 is a block diagram showing the circuit of a phase digital converter according to the digital phase-locked loop compiler in Fig. 2;

[0011] Fig. 4A-4B is a circuit diagram of an up-down converter according to the phase digital converter in Fig. 3 according to one preferred embodiment of this invention; and

[0012] Fig. 5 is a graph showing the phase adjusting values according to the phase digital converter in Fig. 3.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0013] Reference will now be made in detail to the present preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers are used in the drawings and the description to refer to the same or like parts.

[0014] Fig. 2 is a block diagram showing a digital phase-locked loop compiler according to one preferred embodiment of this invention. As shown in Fig. 2, the digital phase-locked loop compiler includes a pre-divider 202, a phase digital converter 204, a digital-to-analog converter 205, a voltage-control oscillator 206, a high-frequency oscillator 208, a post-divider 210, an out-divider 212, and a built-in self-tester 214. Wherein, the pre-divider 202 divides down an input frequency into a comparable input frequency according to a pre adjusting value. The phase digital converter 204 couples with the output of the pre-divider 202 to output a phase-adjusting value according to the comparable input frequency, a feedback frequency, and a sampling frequency. The digital-to-analog voltage converter 205 couples with the output of the phase digital converter 204 to output an adjusting voltage according to the phase adjusting value. The voltage-control oscillator 206 couples with the output of the digital-to-analog voltage converter 205 to output an output frequency according to the adjusting voltage. The high frequency oscillator 208 couples with the input of the phase digital converter 204 to issue a sampling frequency according to the input frequency, the feedback frequency, and the sampling frequency. The post-divider 210 couples with both the input of the phase digital converter 204 and the output of the voltage-control oscillator 206 for dividing down the output frequency into feedback frequency according to a post adjusting value. The out-divider 212, which is

optional, couples with the output of the voltage-control oscillator 206 for dividing down the output frequency into a desired output frequency according to the output adjusting value. The built-in self-tester 214 couples with the output of the phase digital converter 204 to test the phase digital-locked loop according to the phase adjusting value.

[0015] Assume most modules of the voltage-control oscillator 206 operate in frequency ranges from 1MHz ~ 10MHz, 10MHz ~ 100MHz, 100MHz ~ 200MHz, and 200MHz ~ 300MHz etc... However, due to the final output module works in the frequency range 100MHz ~ 200MHz, the frequency range 100MHz ~ 200MHz is selected. In this embodiment, the digital-to-analog voltage converter 205 processes a preset phase adjusting value and outputs the value to the voltage-control oscillator 206. The voltage-control oscillator 206 then outputs an output frequency to the post-divider 210. Upon receiving the frequency, the post-divider 210 automatically divides down the output frequency to a feedback frequency according to the post adjusting value, and further outputs this feedback frequency to the phase digital converter 204. Therefore, if the signal A entering the pre-divider 202 is 30MHz, the pre-divider 202 automatically divides down into a comparable frequency of 1MHz according to the pre adjusting value, and further outputs the comparable frequency to the phase digital converter 204. The sampling frequency from the high frequency oscillator 208 serves to sample the comparable frequency and the feedback frequency, obtained from the above-mentioned phase adjusting value, in the phase digital converter 204. The phase digital converter 204 processes the two sample results to obtain a phase difference, and then converts it to a phase adjusting value. Afterwards, the voltage-control oscillator 206 outputs an output frequency according to the phase adjusting value. These procedures are repeated until the phase of the feedback frequency matches

the phase of the previous comparable frequency. When the phase of the feedback frequency matches the phase of the previous comparable frequency, the built-in self-tester can compare the final phase adjusting value to the preset phase value to judge if the phase-locked loop compiler is working properly.

[0016] According to the first embodiment of the present invention, the phase adjusting value is a 9-bit digital signal and the frequency of the sampling frequency is 360 times of the comparable frequency. Moreover, the pre adjusting value mentioned above can be automatically set by the phase-locked loop compiler according to input frequency and the post adjusting value, and the output adjusting value is set according to the output frequency.

[0017] Fig. 3 is a block diagram showing the phase digital converter according to the digital phase-locked loop compiler in Fig. 2. As shown in Fig. 3, the phase digital converter includes a phase-frequency detector 302, an up-down converter 304, and an arithmetic logic unit 306. Wherein, the phase-frequency detector302 couples with the output of both the pre-divider 202 and post-divider 210 to detect the frequency and phase of the comparable input signal and the feedback signal. The up-down converter 304 couples with the output of both the phase-frequency detector 302 and the high frequency oscillator 208 to output an adjusting signal according to the comparable input frequency, the feedback frequency, and the sampling frequency. The arithmetic logic unit 306 couples with both the up-down converter 304 and the high frequency oscillator 208 to output a phase adjusting value according to the adjusting signal. Whereby, the first embodiment of the up-down converter 304 is shown in Fig. 4A-4B.

[0018] After the phase-frequency detector 302 has detected both the comparable input frequency from the pre-divider 202 and the feedback frequency from the post-divider 210, the high frequency oscillator 208 outputs a sampling frequency to sample the phase of the input frequency and the phase of the feedback frequency. Thereafter, the up-down converter 304 will send out an adjusting signal, and following, the arithmetic logic unit 306 will output a phase adjusting value according to the adjusting signal. Fig. 5 shows a graph of the phase adjusting values according to the circuit in Fig. 3. The arithmetic logic unit 306 generates an input frequency after processing and that is the adjusting value.

[0019] In the digital phase-locked loop compiler of this invention, a high-frequency oscillator 208 is used to provide a sampling frequency to sample of the comparable input frequency and feedback frequency. However the high-frequency oscillator 208 can be external to be shared by other components. Whereby, the frequency of the sampling frequency is 360 times the comparable input frequency because the pre-divider can divide the comparable input frequency as low as 1MHz for higher sampling frequency from the high-frequency oscillator 208. Thereafter, the phases of the input frequency and the feedback frequency are compared to obtain a phase adjusting value. The phase adjusting value indicates any phase shift between the input frequency and the feedback frequency. Hence, the phase-lock conditions can be obtained quickly. Furthermore, this invention also provides a preset phase adjusting value to obtain phase-lock condition in a short period.

[0020] Furthermore, a conventional phase-locked device requires the addition of a analog built-in testing device to perform a self-test. Such an analog built-in testing device is larger in size compared to the digital phase-locked testing device of the present invention

because the analog built-in testing device requires a low-pass filter. As a result, the overall size of the digital phase-locked loop compiler is much smaller.

[0021] In conclusion, the major advantages of this invention includes the following:

1. Feedback phase-locking time is effectively reduced.

2. Without the need to incorporate a large low-pass filter as in an analog phase-locked device, the area is greatly reduced

3.The built-in self-tester is only used for comparing digital signal, therefore, the circuit is relatively simple and requires a small area.

[0022] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.